MALLA REDDY ENGINEERING COLLEGE (AUTONOMOUS)

B.Tech– II year I Sem (MR 20)
II Mid Examination Subjective Question Bank

Subject: Microprocessors and Microcontrollers Fundamentals **Branch: CSE (IOT)**
Name of the faculty: Dr. T. Srinivas Reddy

Instructions:

1. All the questions carry equal marks

2. Solve all the questions

Q.No.	Question	Bloom's Taxonomy Level	CO
	Module III		
1.	How is an interrupt serviced? Outline the interrupt vector table of 8051?	Understand	3
	OR		
2.	Describe the steps for interrupt programming for timers with an example?	Analyze	3
3.	Discuss about 8051 serial port programming with an example?	Analyze	3
	OR		
4.	Explain the concept of timers and counter of 8051 microcontroller with an example?	Analyze	3
	Module IV		
1.	What are the features of MSP430 microcontrollers? Where does the MSP430 fit?	Apply	4
	OR		
2.	Draw and explain functional block diagram of MSP 430 Microcontroller?	Understand	4
3.	Explain in detail about the register set of MSP430 microcontroller?	Understand	4
	OR		
4.	Explain the MSP430 microcontroller addressing modes?	Understand	4
5.	Describe the Instruction set of MSP430 microcontroller?	Understand	4
	OR		
6.	Differentiate FRAM & Flash memories with real time applications?	Analyze	4

7.	What is watchdog timer? Describe its features and applications?	Understand	4
	OR		
8.	Compare MSP430 family of microcontrollers?	Apply	4
	Module V		
1.	With neat diagram explain ADC10 in MSP 430?	Understand	5
	OR		
2.	Explain about comparator used in MSP430 with diagram?	Understand	5
3.	Describe Sigma-Delta ADC in MSP430?	Understand	5
	OR		
4.	Discuss about Edge Aligned PWM used for MSP 430?	Understand	5
5	Interface LCD with MSP 430 microcontroller?	Analyze	5
	OR		
6	Differentiate the types of serial communication methods?	Understand	5
7	Explain the implementation of serial peripheral interface with Universal Serial Communication Interface (USCI) module?	Apply	5
	OR		
8	Describe the Peripherals in MSP430 microcontroller?	Understand	5

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II B.TECH I SEM (MR20, 2020-21 batch) Mid Term Examination-II, February 2022

Objective Questions

Subject: Microprocessors and Microcontrollers Fundamentals (A0450) Max Marks: 20
Branch: IOT Hall Ticket No:

S.No	Questions	Answer
1	What is the clock source for the timers? a) some external crystal applied to the micro-controller for executing the timer b) from the crystal applied to the micro-controller c) through the software d) through programming	B
2	What is the frequency of the clock that is being used as the clock source for the timer? a) some externally applied frequency f ' b) controller's crystal frequency f c) controller's crystal frequency /12 d) externally applied frequency/12	C
3	What is the function of the TMOD register? a) TMOD register is used to set various operation modes of timer/counter b) TMOD register is used to load the count of the timer c) Is the destination or the final register where the result is obtained after the operation of the timer d) Is used to interrupt the timer	A
4	What is the maximum delay that can be generated with the crystal frequency of 22MHz? a) 2978.9 sec b) 0.011 msec c) 11.63 sec d) 2.97 msec	D
5	Auto reload mode is allowed in which mode of the timer? a) Mode 0 b) Mode 1 c) Mode 2 d) Mode 3	C
6	Find out the roll over value for the timer in Mode 0, Mode 1 and Mode 2? a) 00FFH,0FFFH,FFFFH b) 1FFFH,0FFFH,FFFFH c) 1FFFH,FFFFH,00FFH d) 1FFFH,00FFH,FFFFH	C
7	What steps are followed when we need to turn on any timer? a) load the count, start the timer, keep monitoring it, stop the timer b) load the TMOD register, load the count, start the timer, keep monitoring it, stop the timer c) load the TMOD register, start the timer, load the count, keep monitoring it, stop the timer d) none of the mentioned	B
8	If Timer 0 is to be used as a counter, then at what particular pin clock pulse need to be applied? a) P3.3 b) P3.4 c) P3.5 d) P3.6	B
9	In the instruction "MOV TH1,#-3", what is the value that is being loaded in the TH1 register? a) 0xFCH b) 0xFBH c) 0Xfdh d) 0Xfeh	C
10	When an interrupt is enabled, then where does the pointer moves immediately after this interrupt has occurred? a) to the next instruction which is to be executed b) to the first instruction of ISR c) to a fixed location in memory called interrupt vector table d) to the end of the program	C
11	What are the contents of the IE register, when the interrupt of the memory location 0x00 is caused? a) 0xFFHb) 0x00Hc) 0x10Hd) 0xF0H	B
12	After RETI instruction is executed then the pointer will move to which location in the program? a) next interrupt of the interrupt vector table b) immediate next instruction where interrupt is occurred c) next instruction after the RETI in the memory d) none of the mentioned	B

13	Which pin of the external hardware is said to exhibit INT0 interrupt? a) pin no 10 b) pin no 11 c) pin no 12 d) pin no 13	C
14	Which bit of the IE register is used to enable TxD/RxD interrupt? a) IE.D5 b) IE.D2 c) IE.D3 d) IE.D4	D
15	Which of the following combination is the best to enable the external hardware interrupt 0 of the IE register (assuming initially all bits of the IE register are zero)? a) EX0=1 b) EA=1 c) any of the mentioned d) EX0=1 & EA=1	D
16	Why normally LJMP instructions are the topmost lines of the ISR? a) so as to jump to some other location where there is a wider space of memory available to write the codes b) so as to avoid overwriting of other interrupt instructions c) all of the mentioned d) none of the mentioned	C
17	Which register is used to make the interrupt level or an edge triggered pulse? a) TCON b) IE c) IP d) SCON	A
18	What is the correct order of priority that is set after a controller gets reset? a) RI/TI > TF1 > TF0 > INT1 > INT0 b) RI/TI < TF1 < TF0 < INT1 < INT0 c) INT0 > TF0 > INT1 > TF1 > RI/TI d) INT0 < TF0 < INT1 < TF1 < RI/TI	C
19	What should be done if we want to double the baud rate? a) change a bit of the TMOD register b) change a bit of the PCON register c) change a bit of the SCON register d) change a bit of the SBUF register	B
20.	Which of the following registers are not bit addressable? a) SCON b) PCON c) A d) PSW	B
21	Which instruction is used to check the status of a single bit? a) MOV A,P0 b) ADD A,#05H c) JNB PO.0, label d) CLR P0.05H	C
22	To initialize any port as an output port what value is to be given to it? a) 0Xff b) 0x00 c) 0x01 d) A port is by default an output port	D
23	Which of the ports act as the 16 bit address lines for transferring data through it? a) PORT 0 and PORT 1 b) PORT 1 and PORT 2 c) PORT 0 and PORT 2 d) PORT 1 and PORT 3	C
24	Which of the following signal control the flow of data? a) RTS b) DTR c) RTS & DTR d) None of the mentioned	A
25	Which of the following is the logic level understood by the micro-controller/micro-processor? a) TTL logic level b) RS232 logic level c) None of the mentioned d) TTL & RS232 logic level	A
26	In MSP430, the size of the status register is _____ a) 1 byte b) 2 bytes c) 1 bit d) 2 bit	B
27	Which of the following bit/s of the status register that allows the microcontroller to operate in its low power mode? a) Z b) Reserved c) CPU off d) N	C
28	What is actually done to improve the efficiency of a RISC processor? a) instructions are reduced b) they have two or more processors inbuilt connected between c) they have many instructions that are interrelated to each other d) they have one or more registers hard wired to the commonly used values	D
29	To improve the efficiency of an MSP430 based microcontroller, for one register a) there is only one value for all addressing modes b) there are two values for each addressing mode c) there are 2 values for four addressing modes d) there are 4 values for four addressing modes	D

30	There are_____ number of emulated instructions found in the MSP430 a) 4 b) 8 c) 16 d) 24	D
31	.w form is used for operations a) that uses bytes b) that uses words c) that uses both d) that uses none	C
32	Pre increment addressing is available in MSP430? a) true b) false c) can't be said d) depends on the conditions	B
33	Which out of the following is a correct emulated instruction? a) ADC(.B) dst b) ADD(.B) src,dst c) ADDC(.B) src,dst d) AND(.B) src,dst	A
34	dadd instruction can act as _____ a) valid BCD addition b) valid adder with carry c) Both a &b d) none	A
35	Which of the following instructions don't affect the status bits? a) bis b) bic c) bis & bic d) none of the mentioned	C
36	There are _____ number of addressing modes found for the source and _____ number of modes for the destination part. a) 4,4 b) 2,4 c) 7,4 d) 2,2	C
37	MSP430 describes reti instruction as _____ a) Format1 addressing b) Format2 addressing c) Jump addressing d) None of the mentioned	B
38	mov.w R3, R4 takes _____ a) one cycle b) two cycles c) four cycles d) eight cycles	A
39	Indexed addressing can be used for _____ a) source b) destination c) source & destination d) none of the mentioned	C
40	What do you understand form this instruction mov.w X(PC), R6 a) R6 = X+PC b) R6 = PC-X c) R6 = -X-PC d) R6 = -X+PC	A
41	Absolute mode uses which of the following operators? a) % b) / c) $ d) &	D
42	Indirect register mode is used by _____ a) source register b) destination register c)) Both a &b d) none	A
43	Indirect mode and the indirect auto increment mode have which common operator in them a) + b) – c) @ d) &	C
44.	Are the following two instructions similar? MOV @R10,0(R11) and MOV @R10+,0(R11) a) yes b) no c) can't be said d) depends on the conditions	B
45.	MOV @R10,0(R11) is a type of __ a) Register Mode b) Indirect Register Mode c) Immediate Mode d) Indirect increment Mode	B
46	Which instruction is used to call functions? a) MOV b) GO c) CALL d) All of the mentioned	C
47	RET instruction is used for _____ a) determining the end of the program b) for returning back from the subroutine to the main program c) for transferring data from one place to another d) none of the mentioned	B
48	According to conventions being followed, R12 to R15 are used for _____ a) parameter passing b) preserved for call c) all of the mentioned d) none of the mentioned	A
49	We can store the temporary results across a call instruction with the help of which of the following registers. a) R1-R4 b) R4-R11 c) R12-R15 d) All of the mentioned.	B

50	Can we allocate variables on the stack? a) yes b) no c) can't be said d) depends on the conditions	A
51	Which registers are reserved for passing the parameters to a subroutine and then returning the final result? a) R1-R4 b) R4-R11 c) R12-R15 d) All of the mentioned	C
52	What actually is the order of stack frame for a parameter to pass to a subroutine? a) parameter passed to a subroutine b) return address c) saved copies of registers(R4-R11) d) all of the mentioned	D
53	When any subroutine is called, then the first value of stack will be a) value of PC b) the return address c) none of the mentioned d) both are one and the same things	D
54	Which of the following instruction/s is/are used to return back to the main program after the subroutine is completed? a)RET b) RETI c) RET and RETI d) none of the mentioned	C
55	Is the approach of making subroutines effective or not? a) yes b) no c) can't be said d) depends on the conditions	A
56	MSP430 uses vectored interrupts? a) true b) false c) can't be said d) depends on the conditions	A
57	Which of the following is true? a) interrupts are required to wake a CPU from sleep b) same vector address associated with multiple flags c) most interrupts are maskable d) all of the mentioned	D
58	After the interrupt has occurred, the stack is filled with _____ a) return address b) status register c) return address & status register d) none	C
59	What is the purpose of __interrupt () function? a) it is used to enable the interrupt b) it is used to disable the interrupt c) it denotes that the routine is an ISR d) all of the mentioned	C
60	What is the purpose of .intvec assembler directive? a) it creates an interrupt vector entry that points to an interrupt routine name b) one is used for storage, other for display c) one stores locally other stores globally d) the two are the same	A
61	For enabling any interrupt, firstly _____ a) GIE=0 b) GIE=1 c) None of the mentioned d) GIE=0 & 1	B
62	Non maskable vectors are stored at different vector locations? a) true b) false c) can't be said d) depends on the conditions	B
63	Which of the following can generate a non maskable interrupt? a) access violation to flash memory, ACCVIFG b) timer A interrupt c) compare / capture interrupt d) all of the mentioned	A
64	External RST/NMI pin is a nonmaskable interrupt? a) true b) false c) can't be said d) depends on the conditions	A
65	How many cycles are used by MSP430, when reti instruction is executed? a) 3 b) 4 c) 5 d) depends on the conditions	C
66	There are how many MSP430's low power modes available in the chip? a) two b) three c) four d) five	D
67	Which of the following are the low power modes? a) LPM0 b) LPM3 c) LPM4 d) All of the mentioned	D
68	Which of the following modes is also known as the RAM retention mode? a) LPM0 b) LPM3 c) LPM4 d) All of the mentioned	A

69	Waking a device simply means that switching that device's operation from a low power mode to an active mode. a) true b) false c) can't be said d) depends on the conditions	A
70.	Which of the following basic clock modules supplies clock signals to the MSP430? a) ACLK b) MCLK c) SMCLK d) All of the mentioned	D
71	_low_ power_mode_0() states the processor to _____ a) enable the interrupt b) disable the interrupt c) nothing d) to go in an active mode	A
72	More power can be saved by using low_power mode 0 than low_power mode 3. a) true b) false c) can't be said d) depends on the conditions	B
73	BIC_SR_IRQ() is used to _____ a) set the particular bits of the SR b) reset the particular bits of the SR c) any of the above mentioned depending on the conditions d) none of the mentioned	B
74	The only clock that runs in the LPM3 is the _____ a) MCLK b) ACLK c) CLK d) None of the mentioned	B
75	The watchdog counts up and resets the MSP430 when it reaches the limit? a) true b) false c) can't be said d) depends on the conditions	A
76	Which of the following is correct about WDTCTL? a) it is a 16 bit register b) it is guided against accidental writes that require a password c) a reset will occur if a value with an incorrect password is written to WDTCTL d) all of the mentioned	D
77	Which of the following bits reads 0 under normal conditions but goes 1 when it wants to initiate some action? a) WDTNMI b) WDTHOLD c) WDTTMSEL d) WDTCNTCL	D
78	The process of setting the WDTCNTCL bit in WDTCTL is through a) petting b) feeding c) kicking d) all of the mentioned	D
79	WDTIFG flag gets cleared if a) if is interrupt had occurred b) if the interrupt is serviced c) if there can be no interrupt d) all of the mentioned	B
80	Comparator_A+ is controlled by which of the following peripheral registers? a) CACTL1 b) CACTL2 c) CACTL1 & CACTL2 d) None of the mentioned	C
81	CAON bit is used to _____ a) start a timer b) start an A/D conversion c) switch on the comparator module d) switch on the bit transmission	C
82	P2CA4-P2CA0 bits are used for _____ a) giving the power supply to the comparator module b) for selecting the mode of operation of the comparator c) for connecting the non-inverting inputs to the CA0-CA2 pins d) all of the mentioned	C
83	Which of the following bits are not actually associated with the comparator module? a) CAREFx b) CLLDx c) CAON d) CAIFG	B
84	Flag CAIFG is raised, a) at a low level triggered pulse b) at a high level triggered pulse c) at the falling and rising edge of the pulse d) at the falling or rising edge of the pulse	D
85	Which bit is used for exchanging the two inputs of the comparator and invert its output to compensate? a) CAIFG b) CASHORT c) CAPD d) CAEX	D
86	Which of the following is the analog to digital converter that is present in the MSP430 based processors? a) comparator b) successive approximation ADC c) sigma delta ADC d) all of the mentioned	D

87	Higher resolution along with the slow speed is given by which ADC module? a) comparator b) successive approximation ADC c) sigma delta ADC d) all	C
88	The technical terms that help us in differentiating between converters are: a) resolution b) accuracy c) precision d) all of the mentioned	D
89	The number of repeated closeness to the true value is accounted b a) resolution b) accuracy c) precision d) all of the mentioned	C
90	The process of reduction of a continuous input to a discrete output is a) levelling b) signaling c) quantization d) converting	C
91	The intervals between the samples are obtained from _____ a) Fs b) Ts c) Us d) Ks	B
92	The successive approximation converters have a resolution of _____ a) 8-10 bits b) 10-12 bits c) 12-16 bits d) 16-32 bits	B
93	In SAR based conversions, each bit typically requires one clock cycle (sometimes two) to make a comparison and set up the new voltage. a) true b) false c) can't be said d) depends on the conditions	A
94.	The main operations that are basically performed in a SAR ADC are? a) logic to control the operation b) some way of generating the voltages, for comparison c) logic to control the operation and finding some way of generating the voltages for comparison d) none of the mentioned	C
95.	Usually, a capacitor is inserted between an analog input and the ground because a) it blocks the analog voltage b) it suppresses the noise c) it increases the gain d) none of the mentioned	B
96	ADC10 and ADC12 are _____ a) The converters b) SAR modules available in the MSP430 c) Sigma delta modules available in the MSP430 d) Comparator modules available in the MSP430	B
97	ADC10 needs external capacitors on its voltage reference. a) true b) false c) can't be said d) depends on the conditions	B
98	ADC10CTL0 and ADC10CTL1 are registers a) for controlling SAR module b) for controlling the sigma delta module c) for controlling the comparator module d) all of the mentioned	A
99	While conversion is in progress, which of the flag is affected. a) ADC10ON b) ADC10MEM c) ADC10BUSY d) ADC10DF	C
100	ADC10SHTx bits allow_____cycles of the ADC10CLK . a) 4 b) 8 c) 16 d) all of the mentioned	D
101	The input to the ADC10 is selected from_____bits of the ADC10CTL1 register? a) INCHx b) ADC10SC c) ADC10ON d) ENC	A
102	The basic idea behind the sigma delta converter is that a) to carry out the conversion b) to carry out communication c) to reduce the circuit to its simplest way possible and then carry out the conversion d) all of the mentioned	C
103	Sigma delta converter is a _____ a) 1 bit converter b) 2 bit converter c) 3 bit converter d) 4 bit converter	A

104	Sigma delta converter is having good resolution. a) yes b) no c) can't be said d) depends on the conditions	B
105	Here the word sigma represents _____ a) subtraction b) differentiation c) integration d) none of the mentioned	C
106	SD16_A features are controlled by _____ a) memory mapped registers b) register mapped registers c) data mapped registers d) none of the mentioned	A
107	The second part of the ADC handles purely digital signals. a) true b) false c) can't be said d) depends on the conditions	A
108	The second part of the ADC's output is in the form of _____ a) the fast stream of single bits b) the fast stream of multiple bits c) the slow stream of single bits d) the slow stream of multiple bits	D
109	The filtered digital signal is then decimated to a) reduce the rate of samples from fm to fs b) reduce the rate of samples from fs to fm c) increase the rate of samples from fm to fs d) increase the rate of samples from fs to fm	A
110	The SD16 has a second-order modulator with a _____ a) sinc filter b) $sinc^2$ filter c) $sinc^3$ fiter d) rect filter	C
111	SPI a full duplex technique? a) yes b) no c) can't be said d) depends on the conditions	A
112	The concept of SPI is based on _____ a) two counters b) four flip flops c) two shift registers d) four steady state machines	C
113	SPI with the USI can be selected by _____ a) setting the USII2C bit in the register USICTL1 b) clearing the USII2C bit in the register USICTL1 c) setting the USIPE5–7 bits in USICTL0 d) clearing the USIPE5–7 bits in USICTL0	B
114	Transmission and reception are made at a time in SPI? a) true b) false c) can't be said d) depends on the conditions	A
115	When the buffer is _____ the low power mode is_____ a) empty, reset b) having one byte, reset c) full, reset d) empty, two	C
116	Falling edge of the SS pin denotes _____ a) end of the transfer b) starts a new transfer c) selects a new master d) none	B
117	The I2C bus uses which of the following lines? a) CLK b) MISO c) SDA d) All of the mentioned	C
118	I2C is a faster means of data transfer than SPI? a) yes b) no c) depends on the conditions d) can't be said	B
119	Rising edge on SDA while SCL is high denotes _____ a) start condition (S) b) stop condition (P) c) transfer in progress d) none of the mentioned	B
120	Asynchronous serial communication usually requires two wires for each direction plus a common ground. a) true b) false c) can't be said d) depends on the conditions	B
121	In an asynchronous mode of transmission, usually the data is sent along with the a) the start bit b) the stop bit c) the start & stop bit d) none of the mentioned	C
122	Clock is transmitted in the asynchronous communication? a) yes b) no c) can't be said d) depends on the conditions	B
123	There are _____ clocks in the USCI_A a) 1 b) 2 c) 3 d) 4	C

124	What is the non-return to zero format? a) the bits are either high or low and have no gaps between them b) the bits are either high or low and have gaps between them c) the bits are high and have gaps between them d) the bits are low and have no gaps between them	A
125	A framing error occurs is the bit is _____ a) high b) low c) same d) changed	B

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